Abstract

The invention relates to integrated circuits comprising both conductive gates deposited above a semiconductor substrate and a diode is formed between two electrodes. In order to achieve a diode of very small dimensions, the following procedure is adopted: producing the electrodes (ELn, GRST, then thermally oxidizing the electrodes, then exposing the surface of the substrate between the electrodes, then the following operations: depositing doped polycrystalline silicon in order to form one pole of the diode, the substrate forming the other pole,delimiting a desired silicon pattern covering the space left between the electrodes and also covering a region lying outside this space, depositing an insulating layer, locally etching an opening into this insulating layer above the polycrystalline silicon outside the space lying between the electrodes, in order to form an offset contact zone, depositing a metal layer and etching the metal layer.